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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/743,713	05/07/2001	Douglas Philip Turvey	616-034	7323

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EXAMINER
DINH, NGOC V

ART UNIT	PAPER NUMBER
2187	11

DATE MAILED: 08/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/743,713	TURVEY, DOUGLAS PHILIP	
	Examiner	Art Unit	
	NGOC V DINH	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

FINAL REJECTION

1. This Office Action is responsive to Amendment filed 6/30/03 in which claims 1-8, 10-11 are amended.

Applicant's previous arguments are moot with regard to claims 1-11 in view of the new rejection.

Specification

2. The substitute specification filed 06/30/03 has been accepted by the Examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edgar PN 5,440,709

3. As per claims 1, 3, 5:

Edgar teaches a content addressable memory comprising a CAM control logic unit [103, fig. 1, 3; col. 6, lines 24-25] and a plurality of cells connected in a chain, each cell comprising:

a memory block [320, fig. 3] coupled to a common address bus [210, fig. 2]; a comparator [col. 1, lines 62-65] coupled to a common data bus [107, fig. 2] and to the data interface of the memory block;

a switch [113, fig. 5] for coupling the data interface of the memory block with the data bus, and a logic block [324, fig. 3], the memory being operable:

In a Search phase [e.g., match operation] to serially match a sequence of words on the common data bus with the contents of a sequence of addresses in the memory blocks of the cells, the logic block being arranged for cumulatively storing the results of the matching as

the matching proceeds; and in an Access phase [e.g., read/write operation], to render the cells matched in the Search phase serially available for access via the common address and data buses [col. 5, line 1-65; col. 6, lines 19-65; col. 7, lines 7-65; col. 8, lines 35-65].

Implicitly, Edgar teaches a logic block represented as element 324 in figure 3 and the details of which are represented in figure 5 as element 160. Note that figure 5 includes a match flip-flop. This is because in fig. 5, the output of the AND gate 124 is fed back to one of the input of this AND gate [col. 5, lines 63-67], and this is the characteristic of the flip-flop. Furthermore, flip-flop is a well-known circuitry in the content addressable memory designs, there are both combinational logic and storage flip-flops provided on a per word basis, with the storage flip-flops being dedicated to specific functions. The flip-flop contained inside the CAM is used for enabling CAM precharging circuitry or enhancing the speed at which CAM cells can operate. if a match is found in the CAM core, the CAM compare and flip flop in the multimatch buffer associated with the CAM. The CAM array uses a flip-flop with a common control circuit to transfer and refresh data through the flipflop.

4. As per claim 2:

Edgar does not teach a bidirectional switch. However it would have been obvious to one having ordinary skill in the art because the bidirectional switch provides less delay than bus transceivers, which simplifies the control logic required. This also allows the maximum degree of connectivity with the minimum amount of control overhead.

5. As per claims 4-6:

Edgar teaches a content addressable memory (CAM), wherein: several such chips can be chained, in fig. 1 the CAM (103) of the top portion is chained to the CAM (103) of the bottom portion; each chip includes a control unit [106, fig. 1] which can be disabled, and a MASK bus input for determining which bits of the words of the sequence of words are used for matching in the Search phase [col. 6, lines 19-65; col. 10, lines 1-55].

Claims 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edgar PN 5,440,709, and in view of Houseman PN 4, 559,618.

6. As per claim 7:

Edgar does not specifically teach [if not inherent] a CAM including a return line from the end of the chain of cells back to the CAM control unit which changes state when all Match flip-flops in the chain have been accessed.

Houseman further teaches a CAM including a return line [CAM clear 225, fig. 2 from the end of the chain of cells back to the CAM control unit which changes state [e.g., clear operation] when all Match flip-flops in the chain have been accessed [col. 5, lines 51-65; col. 6, lines 3-35col. 10, lines 4-34].

However it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teaching of Houseman into Edgar's CAM. This is because the reset or clear signal on the return line is necessary in order to for all memory cells of CAM to be initialized to 0 state values before and after completion of any matching cycle. Initialization or reset on return line involves storing a logic "0" in all of the memory cells using any known method, such as sequentially writing logic "0" values to each memory cell, or utilizing reset circuitry that resets all of the memory cells simultaneously. This prevents misinterpreted data between matching cycles.

7. As per claims 8 and 11:

Edgar teaches the claimed limitations as noted above.

Edgar does not teach a method of operating a content addressable memory wherein a standard byte address is chosen in all data blocks and a byte different from the inactive state of the data bus is included in that address in every data block. The standard byte address is filled with one data value if the data block in that cell is valid and another date value of the data block in the cell is cleared, ie invalid.

Houseman teaches a method of operating a content addressable memory wherein a standard byte address is chosen in all data blocks and a byte different from the inactive state of the data bus is included in that address in every data block. The standard byte address is filled with one data value if the data block in that cell is valid and another date

value of the data block in the cell is cleared, ie invalid [col. 6, lines 3-35; col. 10, lines 38-60].

It would have been obvious to one having ordinary skill at the time of the invention was made to include the teaching of Houseman into Edgar's CAM. Doing so would increase the reliability of data in the CAM, because the standard byte indicates whether the word contained in the CAM is valid or invalid. An access to the CAM would cause the memory controller to check a validity bit stored in the standard byte to ensure a valid data retrieval . In general, the CAM has an indicator which contains a flag valid/invalid flag indicating whether or not a pertinent word is valid/invalid, a flag (used/free indicator) indicating whether each field in the block is being used or free, and a pointer (block head pointer) indicating the actual position of the memory space matching the flag represented by the pertinent word.

8. **As per claims 9-10:**

Edgar teaches method of operating a content addressable memory wherein each cell is divided into a plurality of distinct data blocks [e.g., slice of input data; abstract; col. 3, lines 35-40].

Edgar does not teach all cells of the CAM including corresponding key fields.

Houseman teaches all cells of the block containing corresponding key fields [col. 1, lines 40-55].

It would have been obvious to one having ordinary skill at the time of the invention was made to include the teaching of Houseman into Edgar's CAM. Doing so would allow fast access to frequently-used value [col. 1, lines 40-65].

CONCLUSION

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc Dinh whose telephone number is (703) 305-3023. The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks, can be reached on (703) 308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

NGOC DINH
Patent Examiner
ART UNIT 2187
July 31, 2003

DONALD A. SPARKS
Supervisor Patent Examiner
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